Large Signal Amplifier

Tyler Parcell

Mitch Belcher

1/19/2016

2/8/2016

I. Objective

To investigate the design and operation of a large-signal bipolar transistor power amplifier for operation in the audio frequency range.

II. Principles of Operation

The amplifier used in this particular lab is a large-signal amplifier. Now there are many different designs for large signal amplifiers present in the world, and no one design is necessarily the best design to use. The "best" design really depends largely on the useage of the amplifier and the contraints in the design process. In this particular lab, the large signal amplifier that was designed and used is componsed of two major parts: a push-pull output stage and differential input stage. Additionally, within the lage-signal output stage, built around the push-pull circuit is a current sink and common-emitter amplifier. Together, all of these pieces form the final design. To better understand this amplifier, we shall trace the circuit from input to output, descirbing exactly what happens. When looking at figure 1, the amplifier, we can see that the small signal input comes in on the left-hand side. It is important to note that this small signal input comes in as a voltage change, not as a current change. From this, the input is fed into the left-side of the differential amplifier. Since the differential amplifier is simply two common-emitter ampifiers, the output of the differential stage is just the difference between this amplified input signal and some constant-amplified bias on the base of the right-side transistor in the differential amplifier. This is the first useful point to note, as doing this allows for an easy way to adjust the "center" point of this amplifier, which might not be as expected due to component imperfections and parasitic effects. This output (of the differential amplifier) is then fed into the current-to-voltage converter above it. This output is then passed to the common-emitter amplifier which acts as the primary input for the large-signal amplifier stage. More specifically, this portion acts as an amplified voltage-to-current converter, manipulating the large biasing current in the large signal branch. This fluctuation of the current in the attached branch on the large-signal amplifier then causes a very large fluctuation (according to the power transistor's beta-values) on the output, which is cimpletely split between the two transistors due to the push-pull operation of the output stage. This is another advantagous point to isolate the large-signal output (each direction) from the rest of the circuit. The two current sinks present then simply act as stabalizers to force the desired current through the circuit where it is needed to obtain the large output requried.

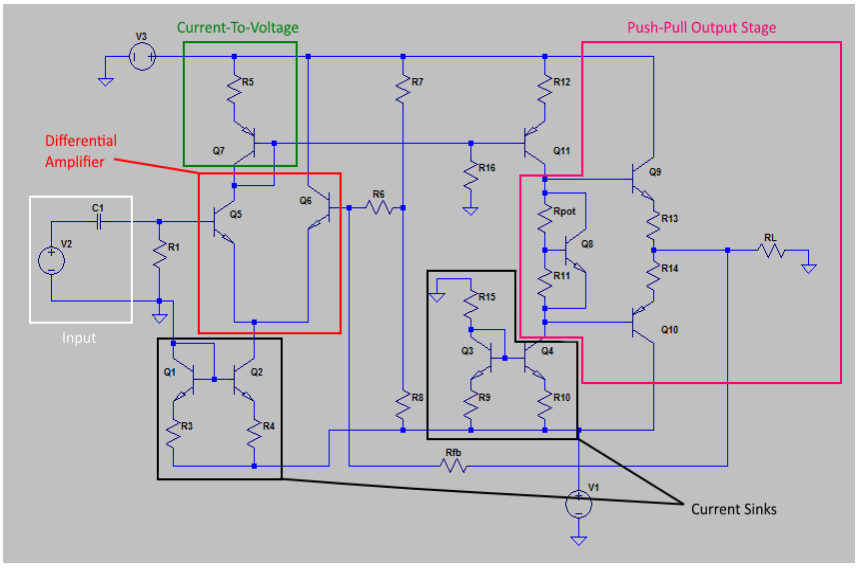

Figure 1: Amplifier layout overview.

Theory

Most of the amplifier's design involved calculations based on simplistic laws such as Ohm's Law or Kirchoff's Voltage/Current Laws. As a result, this section will focus on two main building blocks/concepts present in the design of the amplifier circuit; current sources/sinks and the biasing criteria for this amplifier configuration. Additionally, this section will also cover the importance of matched transistors (with particular consideration with the push-pull output stage) and contain the load-lines for this particular lab's transistors.

i. Current Source/Sink Design

The most general current sink is shown in figure 2 to the right. In general, the goal for this circuit is to draw a desired current in the right-hand branch (referred to as the "operating branch" by this lab report) by using some reference current in the left-hand branch (referred to as the "reference branch" in this lab report). To accomplish this, the total resistance in the reference branch is designed so that, based on the voltage drop across the entire branch, minus the 0.7V from the BJT itself, will yield the desired reference current to maintain. It should be noted that this current does NOT have to be the same as the operating branch's current. To get the desired current out at the operating branch, using this reference current, the voltage drop across Rb2 must match the voltage drop across Rb1. This will happen no matter what, based on Kirchoff's Voltage Law. As a result, variations in Rb2 will result in variations in the current flowing through it. Thus Rb2 must be selected such that the voltage drop set by Rb1, when matched, will force the desired current through the operating branch.

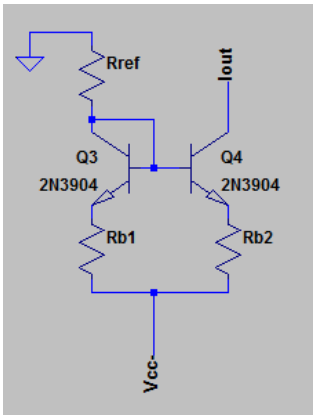

Figure 2: Current Sink.

ii. Biasing Criteria for Circuit

In order for this circuit to be successful there were several DC biasing criteria that needed to be met. Some of these points are highlighted later in the relevant design portion of this report, but ultimately, I would like to highlight the desired DC conditions here and briefly elaborate on their importance to the successful operation of the circuit. All the required conditions are highlighted in figure 3 with the schematic of the circuit. The main reason why this is important is due to the symmetric operation of the final output wave. Having these values off could cause distorted, lops-sided, or low-gain output, depending on which values are incorrect. As a result, these criteria must be met in the final design.

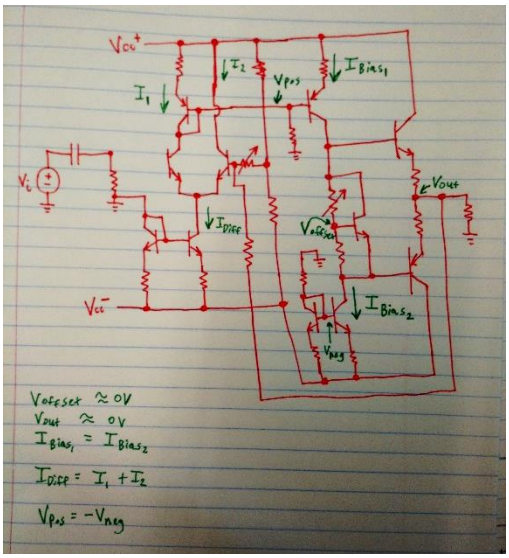

Figure 3: DC Biasing Criteria.

iii. Load Line for Push-Pull Output Stage

The final portion of the theoretical section of this lab report is concerned with the matching of transistors and the load-lines associated with them. The matching of several transistors throughout the entire circuit is definitely a critical aspect to the consistent, undistorted operation of the amplifier as a whole, however, nowhere is this more important than in the output stage. Since the output stage literally reconstructs the desired waveform as two separate halves produced independent of one-another, the matching of the transistors is crucial for an undistorted, symmetric waveform. Unlike various other portions of the circuit, where variations can be fixed using biasing resistors, due to the large swing of the output power transistors, mismatched beta-values become more of an issue. To show the level of matching the two transistors selected for this lab have, two separate load lines were created and overlaid on top one-another for comparison. Thus to determine the actual load line parameters for each, the following deductions must be made, when considering the circuit:

$$V_{CC+} = V_{CE} + 8.1I_E$$

$$\overset{implies}{\Longrightarrow} V_{CC+} = V_{CE} + 8.1\left(\frac{\beta+1}{\beta}\right)I_C$$

$$\overset{implies}{\Longrightarrow} V_{CE} = V_{CC+}|_{I_C=0}$$

$$\overset{implies}{\Longrightarrow} I_C = V_{CC+}\left(\frac{\beta}{8.1(\beta+1)}\right)\Big|_{I_C=0}$$

$$\therefore NPN\ Power\ Transistor\ V_{CE} = 12V$$

$$\therefore NPN\ Power\ Transistor\ I_C = 1.4723A$$

$$\therefore PNP\ Power\ Transistor\ V_{CE} = 12V$$

$$\therefore PNP\ Power\ Transistor\ I_C = 1.4719A$$

As a result, from here we can see that the load lines are basically the same for the two, with less than 1% error between them.

III. Design and Simulation

i. Push-Pull Output Stage

The first circuit designed for the large-signal amplifier was the output stage, which would perform the actual amplification. For this, the push-pull circuit was selected as the base design to build the large-signal amplifier stage off of. The push-pull amplifier stage provides a nice way to control the current on the output by sourcing or sinking current from the output load, making it ideal from an isolation standpoint for the output signal. As a result, the basic push-pull amplifier, shown in figure 4, was first designed. It should be noted that ALL of the device values (i.e. the resistors) were supplied to us, and not calculated. This was due to the limited resources of the lab. The general philosophy behind how they were obtained though was attempting to keep the current in the left-hand branch at around 20mA, while providing an output current of around 1.12A. This forced the values to be about what they are pictured here. In the final design, however, it is desired that no diodes are used. Why is it desired to replace the diodes? Take a look at the following SPICE simulations. The left-hand side ones (figures 5-7) depict how the circuit behaves with the diodes in it. The output waveform is quite nice with minimal distortion. This is definitely much more desirable than the circuit without diodes, which is what figures 8-10 depict. In these figures, it can be seen that there is heavy distortion, especially at lower voltages, due to the "turn-on" voltages of the transistors. Here though, another very important point can be noted. Notice how the distortion is "lop-sided" in that there is minimal distortion on the rising edge versus large distortion on the falling edge. This can be attributed to the mismatched beta-values of the

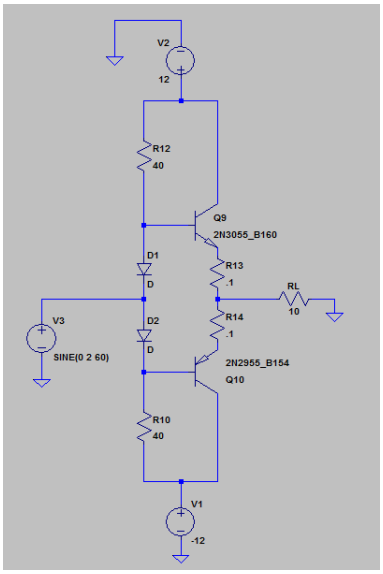

Figure 4: Push Pull Amplifier.

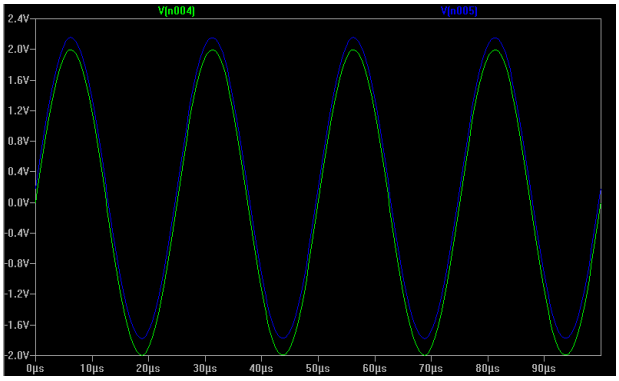

Figure 5: Push Pull Response with Diodes (4Vpp).

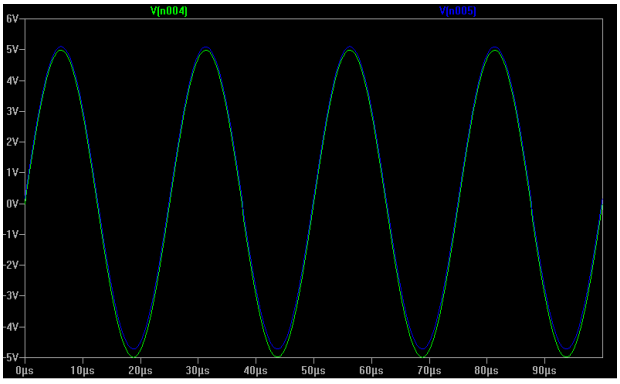

Figure 6: Push Pull Response with Diodes (10Vpp).

transistors used. Since we can't guarantee perfectly matched transistors, it is desirable to replace the diodes with a more sophisticated circuit, to yield a results similar to the case with the diodes, but taking this mismatched transistor aspect into consideration. This addition is then placed in the system in the next section of this report.

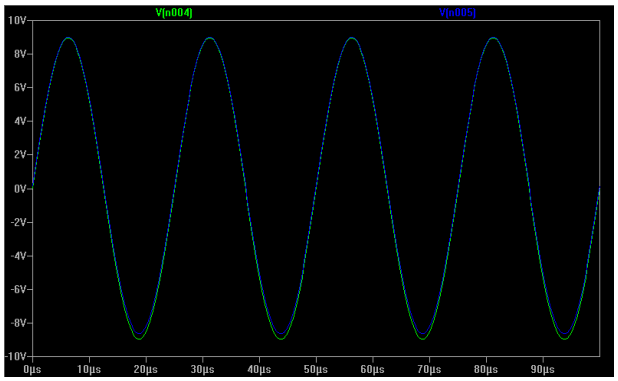

Figure 7: Push Pull Response with Diodes (18Vpp).

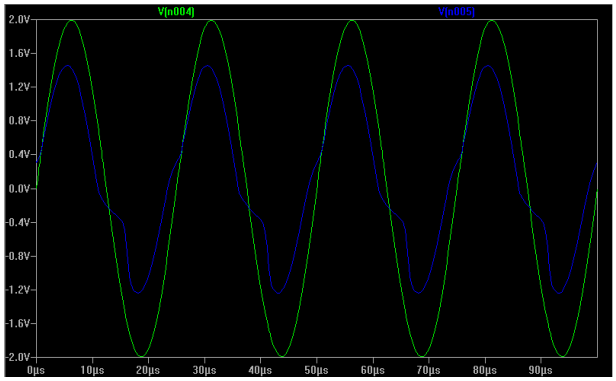

Figure 8: Push Pull Response no Diodes (4Vpp).

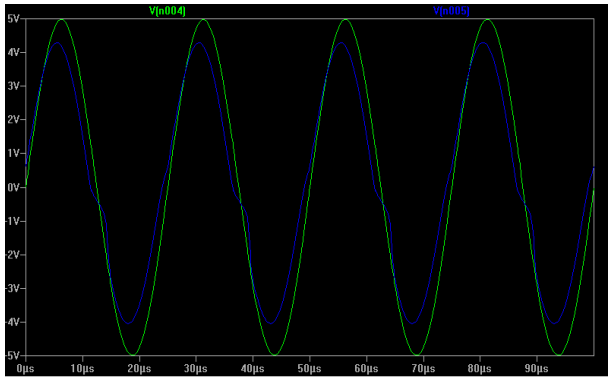

Figure 9: Push Pull Response no Diodes (10Vpp).

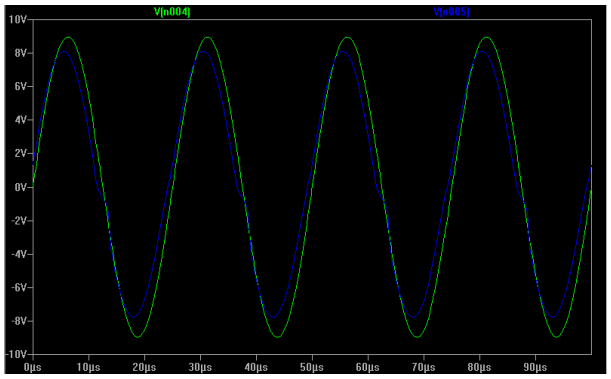

Figure 10: Push Pull Response no Diodes (18Vpp).

ii. Push-Pull Large Signal Amplifier Stage

The next portion of the large signal amplifier design was to improve the push-pull stage to actually supply gain to the input signal by manipulating the current in the right-hand branch, as depicted in the circuit in figure 11. To accomplish this, several changes were made to the original push-pull amplifier stage design. The first modification was to add the Q8 transistor in addition to two 100Ω resistors to adjust the offset in the biasing voltages for the base of the two output power transistors. This was the desired

modification that was previously mentioned in this same section as a replacement for the biasing diodes. The next modification was to add a current sink to the base of the left-hand side branch to force the desired current to be pulled through there for adequate gain (and suitable output current). Figure 2 shows the basic design to a current sink/source. In this particular case, the desire was to have the reference branch be at approximately 1mA, while the working branch will be at about 20mA. To accomplish this, the current in the left-hand branch of the current sink had to be designed to draw a total current of around 1mA. This, along with the given voltage from of 12V, yields us the following:

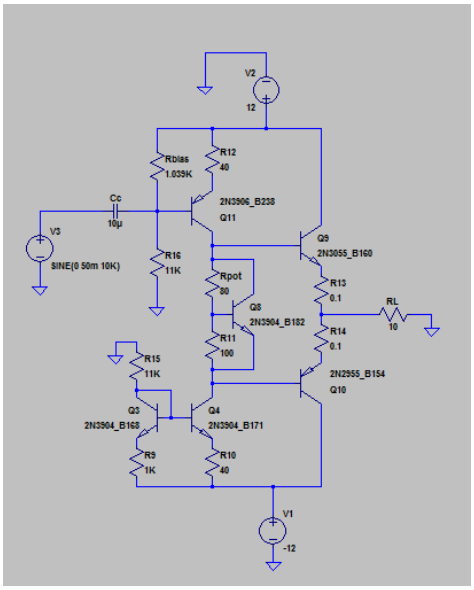

Figure 11: Full Large Signal Stage

$$R_{total} = \frac{12}{0.001} = 12000\Omega = 12K\Omega$$

With that in mind, the final requirement, to get the current sink to draw the desired current on the right-hand branch, the voltage drop across the emitter resistance of the reference branch had to match, exactly, that of the operating branch, this would force the same voltage drop across the operating branch's resistor, forcing it to draw the desired current to make it happen. Since, at the desired current, the operating branch was to drop about 1V, this gave:

$$R_9 = \frac{1}{0.001} = 1000\Omega = 1K\Omega$$

$$\xrightarrow{implies} R_{10} = 10K\Omega$$

The next critical component design required for this large-signal amplifier was the input stage for it, which essentially consisted of a common-emitter amplifier used to convert changes in the base-voltage to changes in the connected branch's current. The design here ultimately required that the base-voltage of the transistor be DC biased to about the same voltage as the mirrored point on the lower-half of the circuit in the current sink. This voltage was approximately 10.4V (1V + 0.7V from the -12V supply rail). Logically, this point should then thus be biased the same as the bottom point, yielding the requirement that the resistors be as follows:

$$R_{Bias} \approx 1K\Omega$$
$$R_{16} \approx 10K\Omega$$

This completes the design phase for the large-signal amplifier output stage for the amplifier circuit. With this, a frequency response was then conducted in SPICE to verify that the circuit was operating as expected. These results can be seen in figure 12.

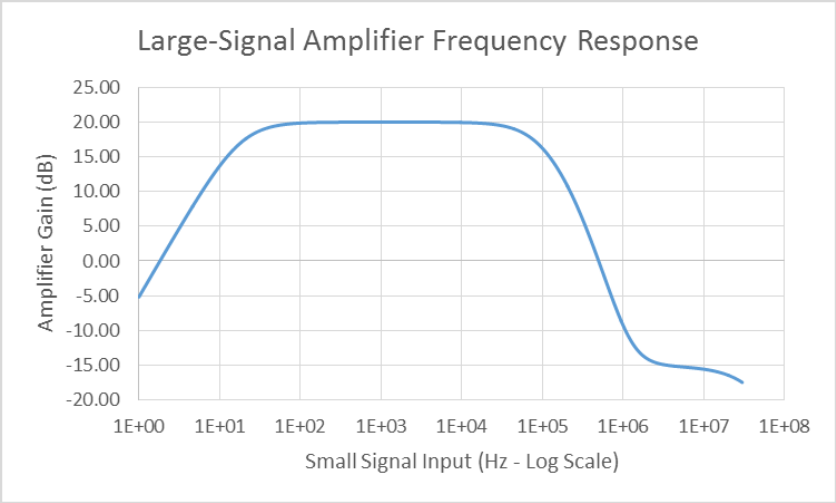

Figure 12: Large Signal Amplifier Frequency Response (SPICE)

iii. Differential Amplifier Input Stage

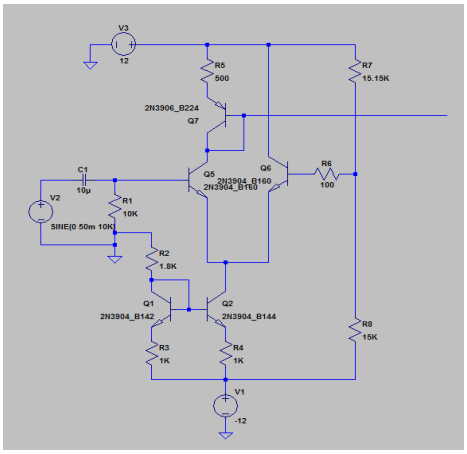

Figure 13: Full Small Signal Stage

The next part of the circuit that needed to be designed was the small-signal input stage which is based off of a differential amplifier. The advantage to using a differential amplifier is the use of two inputs for determining the output voltage. This use allows us to set the "zero" point for the amplifier configuration, which is also the same location where the feedback will be placed to help control the gain. This particular version of the circuit, as shown in figure 13 is quite simplistic, and has minimal biasing resistor networks, making its overall design process fairly straight-forward. The first noticeable section on the amplifier design is the current sink located at the bottom of the differential amplifier. Based on the desired specifications, this current sink was desired to have a 4mA draw on the operating branch with a 4mA reference on the reference branch; essentially we want a current mirror. To accomplish this, a fixed voltage drop of about 4V was set for the reference branch across the emitter resistor. This meant that the resistor itself would be:

$$R_3 = \frac{4}{0.004} = 1000\Omega = 1K\Omega$$

Since the entire voltage drop across the reference branch needed to be 12V (from ground to -12V), and now 1.7V are accounted for (1V from the emitter resistor and 0.7V from the transistor, due to the collector-base terminals being tied together), this yields a collector biasing resistor of:

$$R_2 = \frac{12 - 4.7}{0.004} = 1825\Omega \approx 1.8K\Omega$$

Finally, to continue with the desired specifications of the current-mirror, the emitter resistor on the operating branch must match that of the reference branch, since the voltage drop across that point must be the same, forcing the same current through it. Thus we get:

$$R_4 = 1K\Omega$$

The next importance piece to the differential amplifier design is the output section, which essentially consists of a transistor connected in such a way as to act as a current-to-voltage converter. To do this, the BJT, in this case Q7, must be connected as shown in the circuit. This will cause the current change in the emitter-collector pathway to yield a voltage change on the base terminal. Since the final goal will be to connect this terminal to the input terminal of the previously design large-signal amplifier stage's input terminal via DC coupling, it is absolutely critical that their DC biasing points match. This means that the collector-emitter branch, which will have a total of 2mA flowing through it, will require a collector resistor of:

$$R_5 = \frac{12 - 10.4 - 0.7}{0.002} = 450\Omega$$

Due to variations in components, however, this will likely be a potentiometer to allow the resistor to vary around this point. Finally, as for the biasing network for the right-hand side of the differential amplifier, stiff-biasing criteria was used, albeit incorrectly, to obtain the two approximately 15KΩ values. The truth is, of course, that these values don't matter too much so long as they are similar, to yield a near 0V DC biasing voltage at the base of that BJT (Q6). The slightly higher top resistor for this network was obtained through trial and error to help center the output about the desired DC biasing point to yield a minimally distorted sign-curve output. Once complete, the circuit was simulated and a frequency response was conducted. These results can be seen in figure 14.

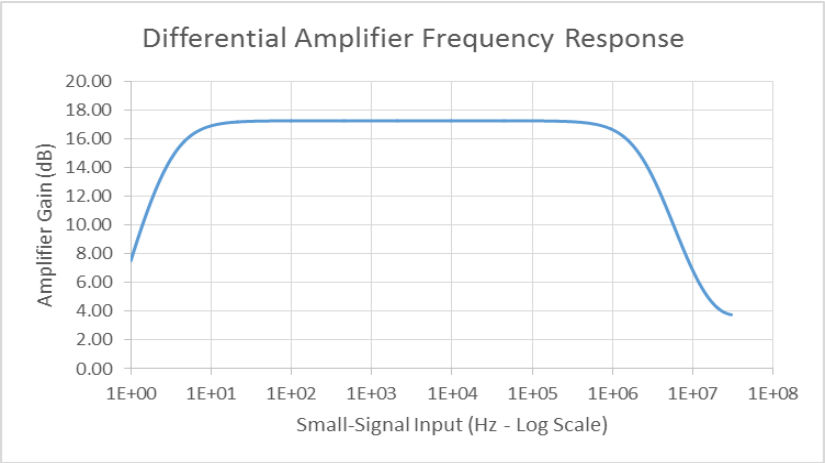

Figure 14: Differential Amplifier Frequency Response

iv. Completed Large-Signal Amplifier Design

The final step in the design process was to consider the combination of the two circuits to yield a large signal amplifier. Since there is little design to be completed here, the two circuits were simply connected together, and a SPICE simulation was run to determine how the entire circuit would behave. This circuit is shown in figure 15 and the complete frequency response of it from within SPICE is shown in figure 16. It should be noted that there were some specification changes, such as the 6V supply rails instead of the 12V ones. This change, along with a few other minor ones, are highlighted in the conclusion section of this report.

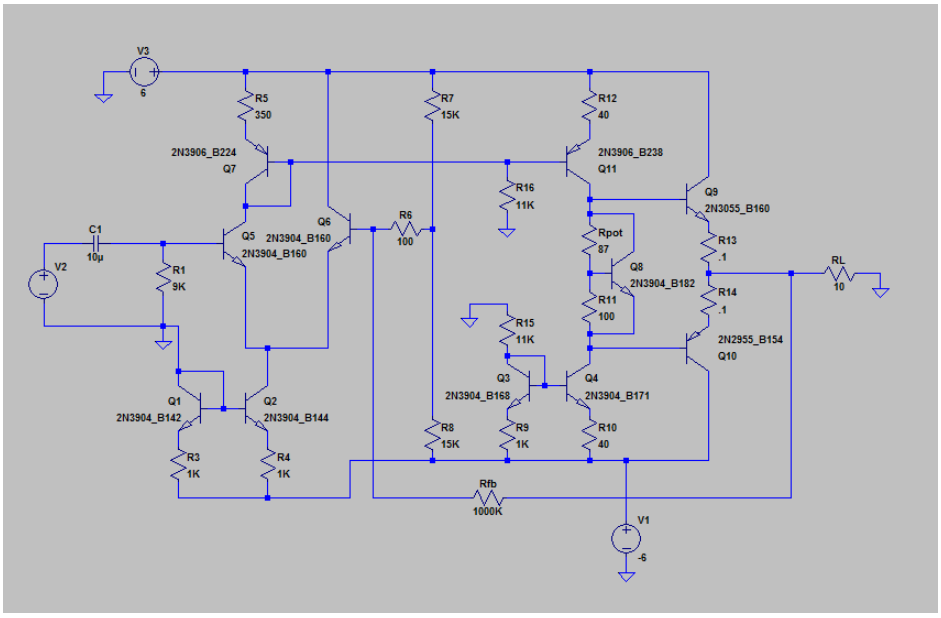

Figure 15: Complete Large Signal Amplifier Design.

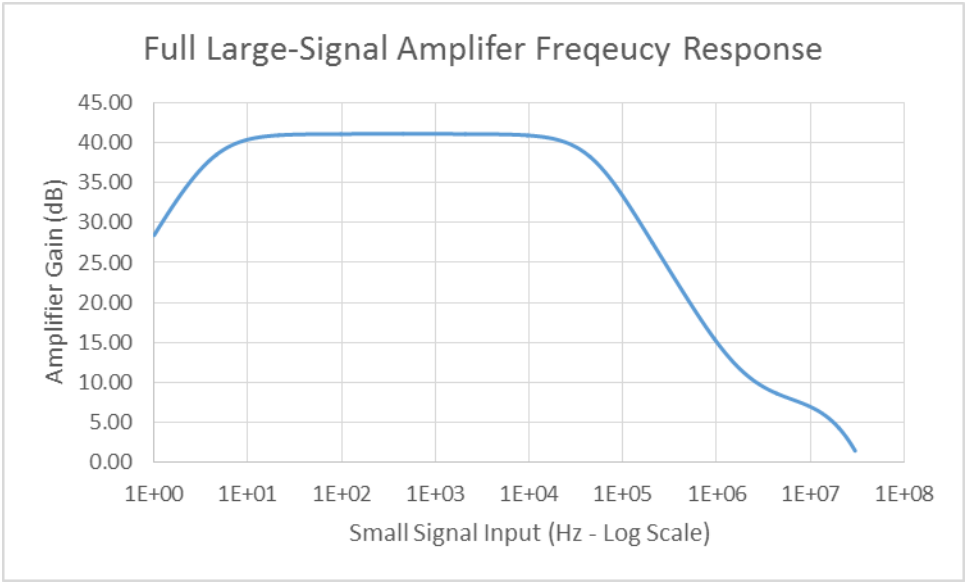

Figure 16: Full Large Signal Amplifier Frequency Response.

IV. Device Characteristics

See all attached Curve-tracers in the "appendices" for this portion of the lab report.

V. Test Results

i. Component and Measurements

When it came to the actual in-lab portion, various components were selected based on their overall availability and standard values. This meant that many resistors were modified slightly while remaining within the desired tolerances. These components were then measured multiple times to ensure a better understanding of the values used.

Measured Component Values				
Resistors	**Measurements**			**Averages**
R1 (kΩ)	8.69	8.69	8.69	**8.69**
R2 (kΩ)	Not used			
R3 (kΩ)	1.03	1.03	1.03	**1.03**
R4 (kΩ)	0.99	0.99	0.99	**0.99**
R5 (Ω)	359.00	358.00	359.00	**358.67**
R6 (Ω)	100.23	99.00	100.10	**99.78**
R7 (kΩ)	14.90	14.80	14.92	**14.87**
R8 (kΩ)	14.92	14.92	14.90	**14.91**
R9 (Ω)	994.00	993.80	995.00	**994.27**
R10 (Ω)	39.02	39.02	39.00	**39.01**
R11 (Ω)	98.90	98.80	99.00	**98.90**
R12 (Ω)	998.00	997.00	998.20	**997.73**
R13 (Ω)	0.15	0.15	1.45	**0.58**
R14 (Ω)	0.15	0.15	0.14	**0.15**
R15 (kΩ)	10.81	10.80	10.82	**10.81**
R16 (kΩ)	10.78	10.80	10.79	**10.79**
Rload (Ω)	9.96	9.95	9.96	**9.96**
Rfeedback (MΩ)	1.04	1.04	1.04	**1.04**
Pot1 (Ω)	992.00	993.00	990.00	**991.67**
Pot2 (Ω)	86.90	88.00	87.00	**87.30**
Pot3 (kΩ)	4.84	4.83	4.80	**4.82**
Capacitors	**Measurements**			**Averages**
Cc1 (μF)	9.54	9.54	9.53	**9.54**

Table 1: Component Measurements.

Measured Beta Values		
Transistor	**Type**	**Beta**
Q1	NPN	142
Q2	NPN	144
Q3	NPN	168
Q4	NPN	171
Q5	NPN	160
Q6	NPN	160
Q7	PNP	224
Q8	NPN	182
Q9	NPN	160
Q10	PNP	154
Q11	PNP	238

Table 2: BJT Beta Values

ii. Push-Pull Output Stage Test Results

The first part of the in-lab experimentation began with the implementation of the basic push-pull amplifier design with the inclusion of diodes to provide the transistor base voltage biasing. Similar to the SPICE simulations presented in the earlier, design section of this report, there were six experiments that were conducted on this circuit; with diodes for biasing the transistors at the 4Vpp, 10Vpp, and 18Vpp levels and no diodes present for the transistor biasing at the same 4Vpp, 10Vpp and 18Vpp levels. These results are shown in figures17-22 on the next page.

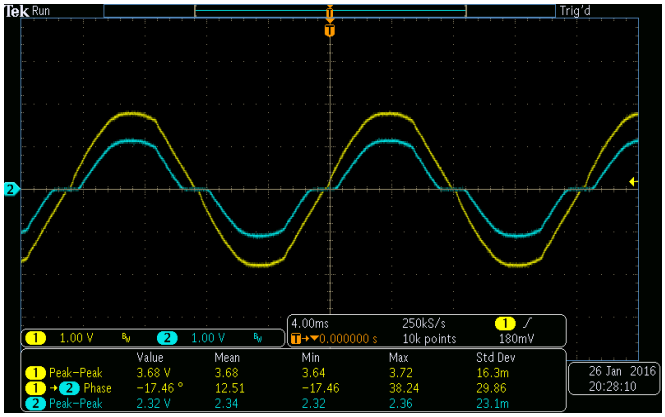

Figure 17: Push-Pull Response without Diodes (4Vpp).

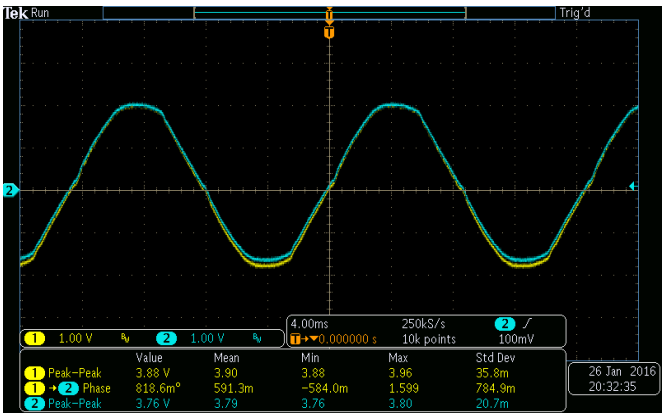

Figure 18: Push-Pull Response with Diodes (4Vpp).

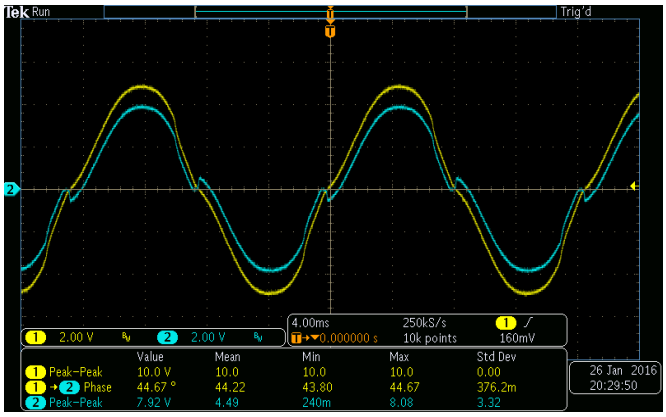

Figure 19: Push-Pull Response without Diodes (10Vpp).

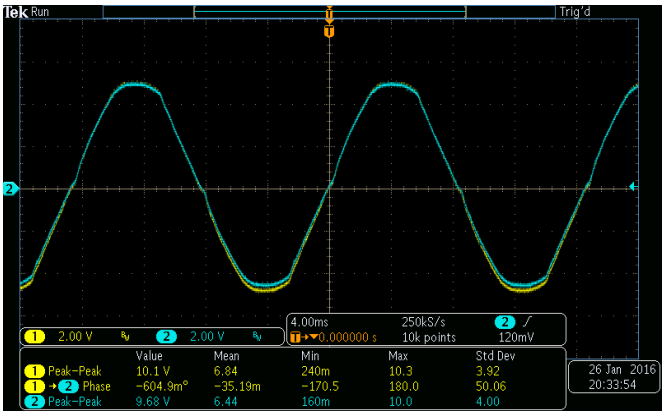

Figure 20: Push-Pull Response with Diodes (10Vpp).

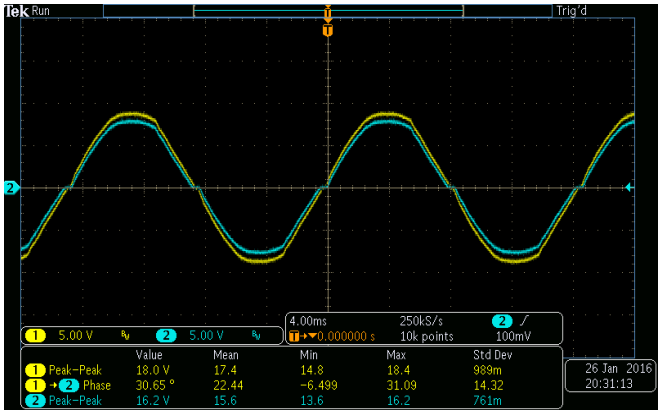

Figure 21: Push-Pull Response without Diodes (18Vpp).

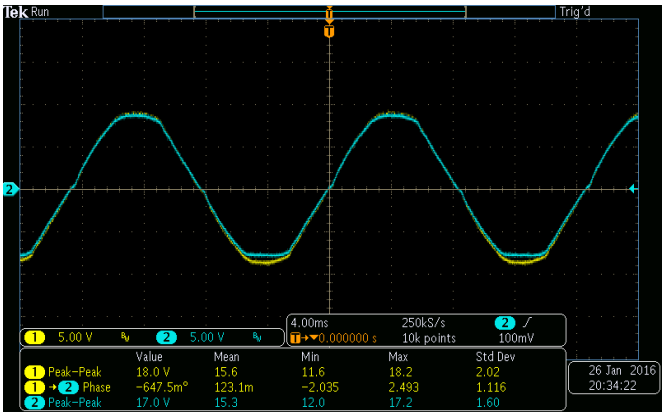

Figure 22: Push-Pull Response with Diodes (18Vpp).

iii. Push-Pull Large Signal Output Stage Test Results

Once the push-pull output stage was assembled, it was modified to fulfill the desired requirements of the large signal amplifier stage; that is, according to the design specifications, the addition of the current source/sinks and amplifier input for current variations in the left-hand branch of the output stage. This was done according to the design portion of this report. The actual in-lab experimentation that occurred for this particular stage of the amplifier circuit involved both a full frequency response and a triangular wave distortion analysis transient response. The full frequency response can be seen in figure 23 and the triangular wave distortion test can be seen in figure 24. The primary goal of the triangular response was to indicate how the beta-related current gain varies with voltage changes on the transistor's base. As the plot shows, the output is "rounded" indicating that there is some signal distortion at the upper-ends of the amplifier's operating conditions. The frequency response of the circuit is of particular interest, as it is quite narrow here, as shown, but, as we add stages, the bandwidth will change quite a bit, so it is interesting to note this fact here.

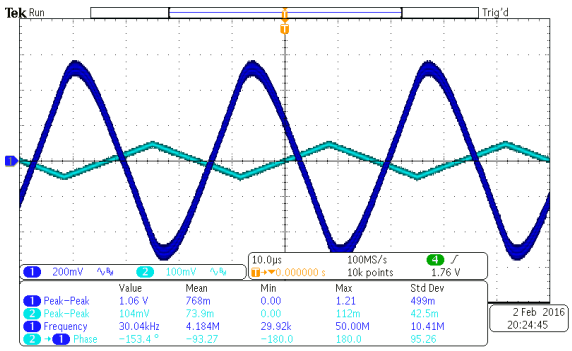

Figure 23: Push-Pull Triangular Response.

Power Stage Frequency Response (Input @ 100 mV)		
Frequency (Hz)	**Output Voltage (V)**	**Gain (dB)**
5.0E+02	0.34	10.53
1.0E+03	0.64	16.12
2.2E+03	0.98	19.79
3.0E+03	1.08	20.67
7.0E+03	1.30	22.28
1.0E+04	1.38	22.80
3.0E+04	1.38	22.80
4.0E+04	1.14	21.14
5.1E+04	0.98	19.79
6.0E+04	0.86	18.65
1.0E+05	0.56	14.96
2.0E+05	0.30	9.54

Table 3: Power Stage Frequency Response Data.

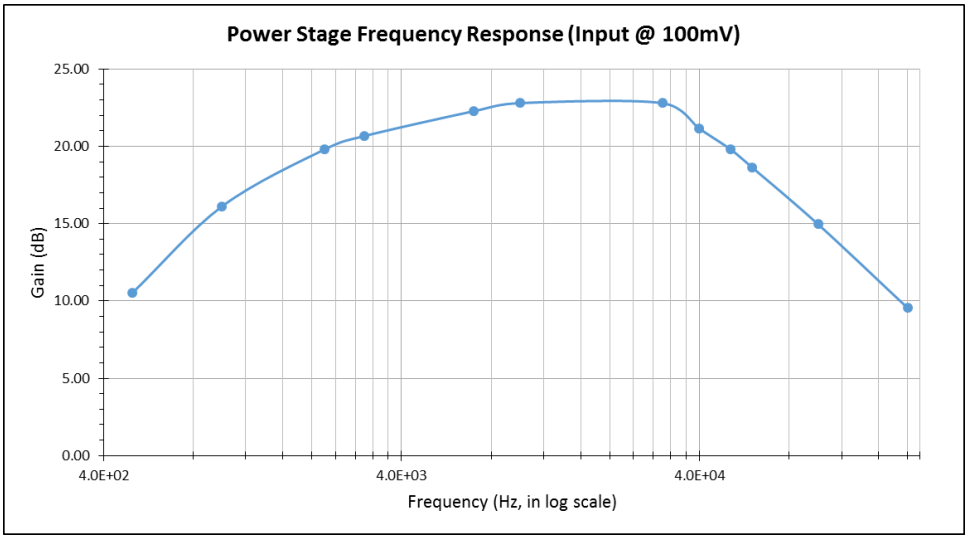

Figure 24: Power Stage Frequency Response.

iv. Differential Amplifier Input Stage Test Results

The final piece to the puzzle that is the large signal amplifier is the small-signal differential amplifier input stage. This stage is responsible for taking the small input signal, which is a variation in the voltage applied, and the turn that into a precise voltage change while taking into consideration desired feedback characteristics (offsetting the "zero" point of the circuit). It is also necessary to provide the required current to actually drive the large output current desired from the large-signal amplifier due to the built in current sources/sinks for a consistent, reliable performance. This stage was again, designed in consideration of the design portion of this report, and a full frequency response was conducted on it in lab for use when combining it with the large-signal output stage. The voltage-transfer characteristics/frequency response can be seen in figure 25, and matches quite nicely with its corresponding SPICE simulation. As with the previous portion of the circuit (the large signal stage) it should be interesting to note the actual range of operation this amplifier has in its frequency response, and how that range of operation compares with the final amplifier design in the next section of the results portion of this lab.

Differential Stage Frequency Response (Input @ 100 mV)		
Frequency (Hz)	Output Voltage (V)	Gain (dB)
1.0E+02	0.53	14.45
1.0E+03	0.53	14.45
1.0E+04	0.53	14.45
5.0E+04	0.52	14.32
5.0E+05	0.51	14.19
1.0E+06	0.49	13.77
3.0E+06	0.38	11.50
3.2E+06	0.36	11.17
4.0E+06	0.34	10.53
7.0E+06	0.28	8.94
3.0E+07	0.11	0.51

Table 4: Differential Stage Frequency Response.

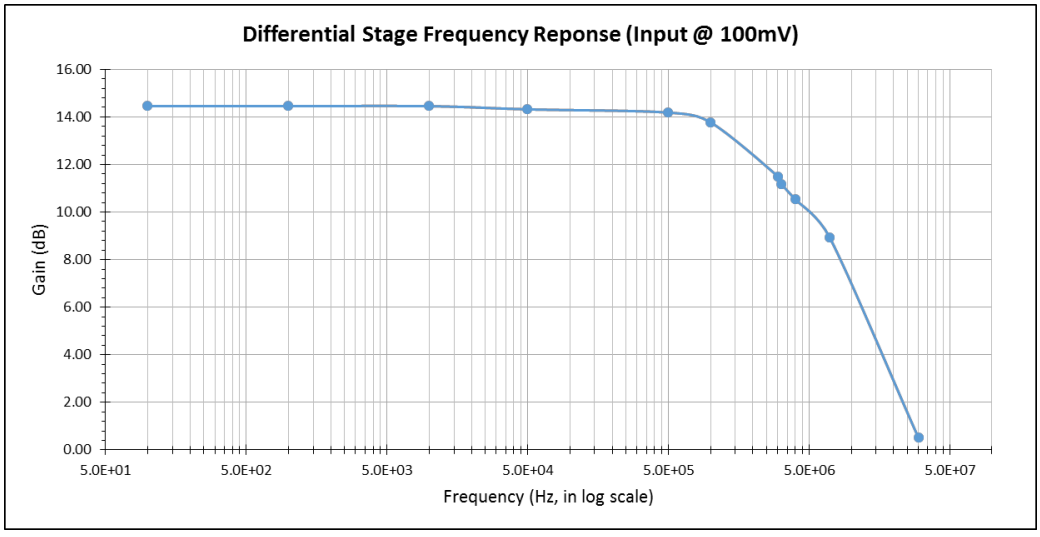

Figure 25: Differential Stage Frequency Response.

v. Completed Large Signal Amplifier Test Results

Combining the two halves of the circuit together involved a small process of AC and DC coupling considerations. To begin, the two stages were first to be attached while being AC coupled, that way the variations in the DC biasing criteria of the two individual circuits wouldn't cause any parasitic effects to the other's operation. This, however, does require the use of a coupling capacitor, which has its own associated parasitic effects to the low-corner of the frequency response. Shown in figure 26 is the frequency response of the two circuit's being AC coupled with a 10µF capacitor. The plot clearly indicates the parasitic effect of this capacitor, which the sharp attenuation at the low-corner frequency of the response.

AC Coupled Frequency Response (Input @ 30 mV)		
Frequency (Hz)	Output Voltage (V)	Gain (dB)
2.0E+00	0.72	27.60
1.7E+01	5.12	44.64
3.0E+01	5.44	45.17
1.0E+02	5.60	45.42
5.0E+02	5.60	45.42
1.0E+03	5.68	45.54
7.0E+03	5.84	45.79
2.0E+04	6.00	46.02
3.0E+04	6.00	46.02
4.0E+04	6.08	46.14
5.0E+04	5.84	45.79
6.0E+04	5.68	45.54
7.0E+04	5.12	44.64
8.0E+04	4.32	43.17
1.0E+05	3.24	40.67
2.0E+05	1.24	32.33
5.0E+05	0.5	24.44

Table 5: AC Coupled Frequency Response

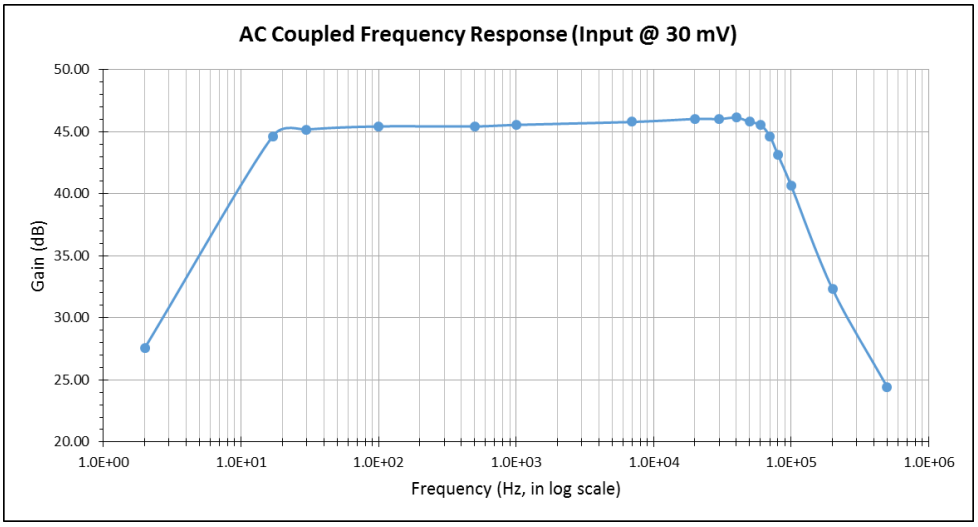

Figure 26: AC Coupled Frequency Response.

The next test for the combination of the two circuits was to ensure that the connection point, which again was according to the specified schematic in the design portion of the lab, matched DC operating points within a few mV. Since our circuit met this criteria, the two circuits were then able to be joined together without the need for the coupling

capacitor. The same frequency response was then performed on this circuit, and the results can be seen in figure 27. As the figure shows, the low-corner frequency is about the same, as far as the position is concerned. Additionally, the gain is very comparable to the AC coupled version. Since, however, we removed the internal coupling capacitor, the actual attenuation at this low-corner frequency is much smaller. It is still present, however, due to the coupling capacitor on the input of the circuit itself.

DC Coupled Frequency Response (Input @ 30 mV)		
Frequency (Hz)	Output Voltage (V)	Gain (dB)
2.0E+00	2.88	39.65
1.7E+01	6.16	46.25
3.0E+01	6.40	46.58
1.0E+02	6.48	46.69
5.0E+02	6.56	46.80
1.0E+03	6.56	46.80
7.0E+03	6.64	46.90
2.0E+04	6.72	47.00
3.0E+04	6.80	47.11
4.0E+04	7.12	47.51
5.0E+04	6.72	47.00
6.0E+04	6.00	46.02
7.0E+04	5.12	44.64
8.0E+04	4.48	43.48
1.0E+05	3.28	40.78
2.0E+05	1.18	31.90
5.0E+05	0.45	23.52

Table 6: DC Coupled Frequency Response.

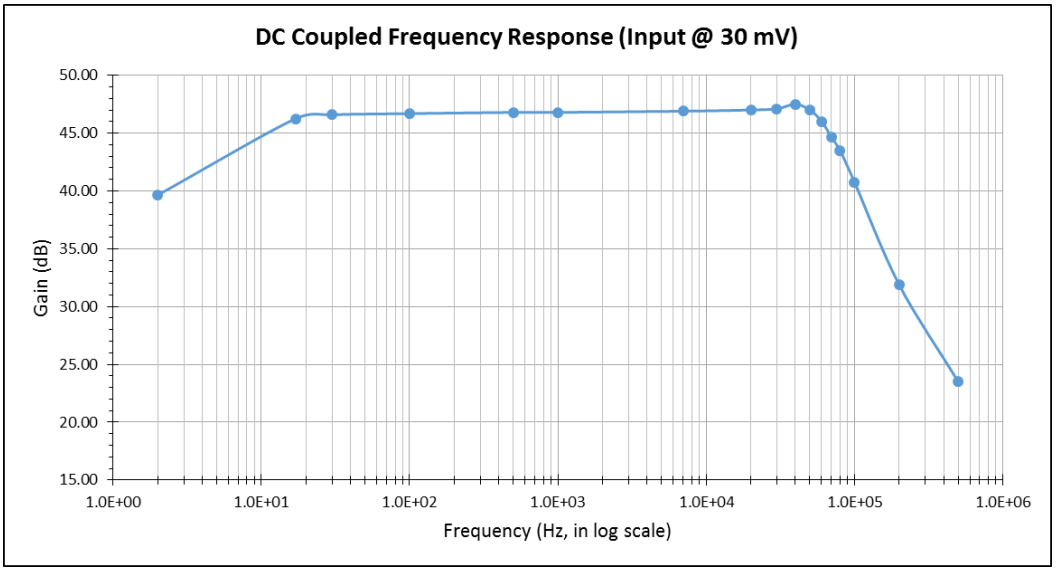

Figure 27: DC Coupled Frequency Response.

Upon connecting the two halves together in a DC coupled fashion, there were an array of other tests performed to determine the characteristics of the circuit's operation. The first thing that was completed was the addition of feedback and bypassing emitter resistance on the input amplifier configuration to the power amplifier stage. In this case, the feedback resistance that was added was 1MΩ. The reason this was chosen as the feedback resistance was to limit the amount of gain-cutting it did while increasing stability. The desire to reduce gain cutting was in favor of meeting the desired

specifications for the lab itself. The frequency response of the new amplifier with the feedback and bypass capacitor is shown in figure 28. As the plot (and data) show, while the feedback resistor did cut back on the gain a bit, when combined with the bypass capacitor, the overall gain increased a little bit, allowing the circuit to come much closer to achieving the desired specifications. As to whether the specifications were actually met or not is discussed later in the conclusion portion of this lab report.

Feedback Amp Frequency Response (Input @ 30 mV)		
Frequency (Hz)	Output Voltage (V)	Gain (dB)
2.0E+00	4.48	43.48
4.0E+00	6.72	47.00
1.7E+01	8.72	49.27
3.0E+01	8.88	49.43
1.0E+02	8.96	49.50
5.0E+02	8.96	49.50
1.0E+03	8.96	49.50
7.0E+03	8.96	49.50
2.0E+04	9.04	49.58
3.0E+04	9.20	49.73
4.0E+04	9.44	49.96
5.0E+04	9.20	49.73
6.0E+04	8.56	49.11
7.0E+04	7.84	48.34
8.0E+04	6.72	47.00
1.0E+05	5.12	44.64
1.5E+05	2.4	38.06
2.0E+05	2.08	36.82
5.0E+05	0.76	28.07

Table 7: Feedback Frequency Response.

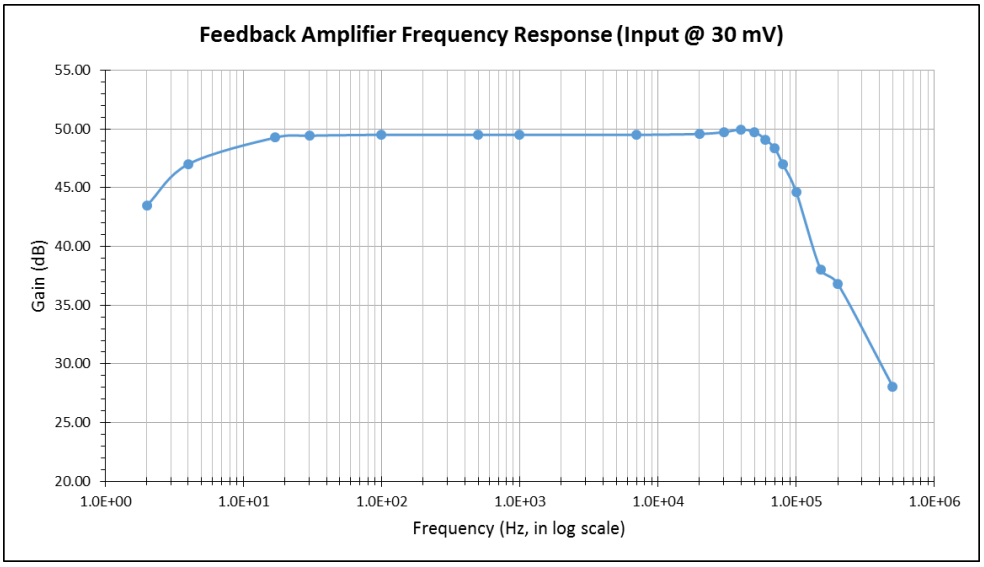

Figure 28: Feedback Amplifier Frequency Response.

With the amplifier operating quite nicely, and as anticipated, two more tests were conducted to better understand its operating characteristics. The first test was another triangular wave input to deduce the amount of distortion in the amplifiers output. Since the amplifier is really pushing quite close to the power rails (at 6V for this portion of the lab – see the conclusion for more details as to why this changed), heavy distortion was

definitely expected. Figure 29 below shows us that, while there definitely was distortion, it wasn't terrible.

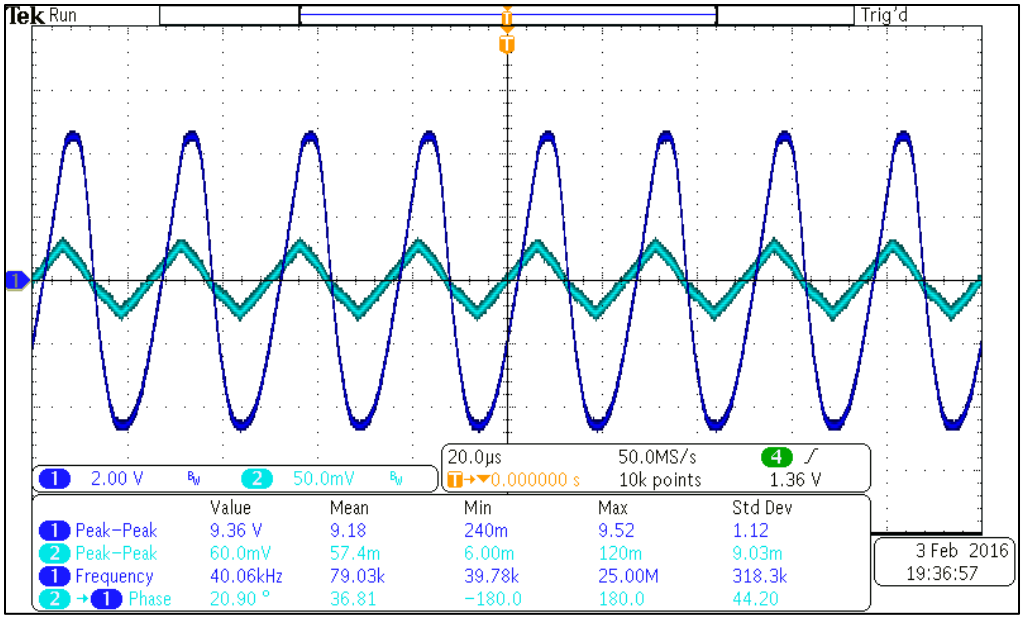

Figure 29: Full Amplifier Triangular Response.

The final test conducted in this lab with the completed circuit was a square-wave input to evaluate the rise and fall time of the circuit. This would actually allow for the deduction on the high-corner frequency as an additional verification metric for the operating characteristics of the circuit. Figure 30 and 31 shows the square-wave response at both the 1KHz input frequency and the 5KHz input frequency. From this, it can be shown that the rise time was approximately 3.6µS and 5.6µS (1KHz and 5KHz respectively) and the fall time was approximately the same for both. This yields:

$$f_H = \frac{0.35}{RiseTime} = \frac{0.35}{\left(\frac{3.6\mu S + 5.6\mu S}{2}\right)} = 76KHz$$

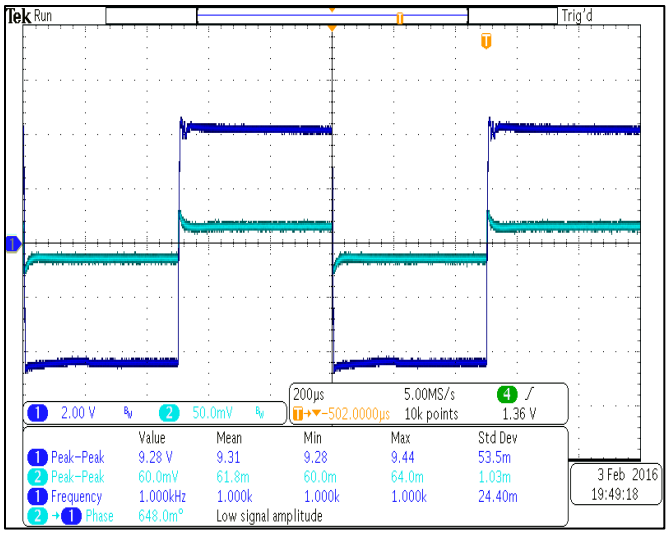

Figure 30: Full Amplifier Square-Wave Response (1KHz)

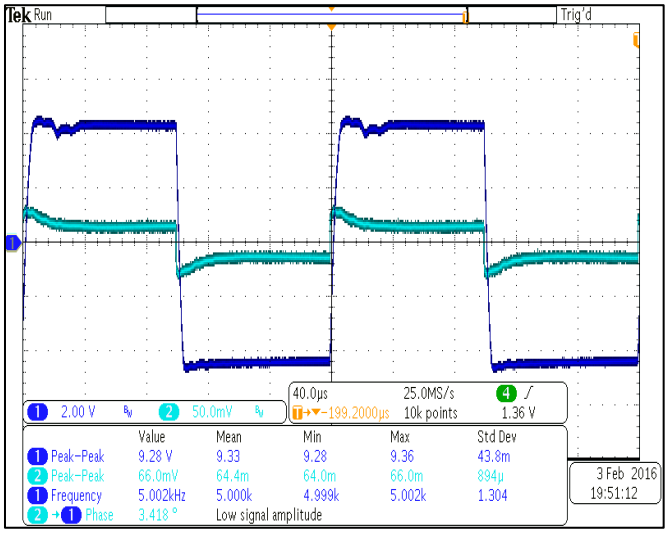

Figure 31: Full Amplifier Square-Wave Response (5KHz)

VI. Conclusion

Overall, this lab was very successful at displaying the concepts that drive multistage amplifier design in the context of a large-signal amplifier. The lab setup to make students understand that by combining different, known circuits, a single amplifier can be created to accomplish a desired task. In this case, that task was comparable to an audio amplifier, which must take a small-voltage-signal input and produce a large-power output; the goal was 5W. There were however snags that were hit during the execution of this lab and limitations in lab equipment at our disposal. As a result, this conclusion will be slip up into two other major sections. Firstly, the flow of the lab itself, mainly from a design perspective, and then a "problems faced" section, and what was done to remedy the situation.

Firstly, the design of this circuit was quite daunting at first to say the least. The amplifier design was considerably more complicated circuit than one we've ever had to design before. That being said though, like any engineering student should, the most successful way our group (myself and my lab partner) designed the circuit was by breaking the circuit up into several pieces, as outlined in the principles of operation section. This meant that the design of independent sections excluded the effects of other sections. This, while logical, does impose the possibility of conflicting DC biasing conditions, but those were kept in consideration, and crucial to the design of successive pieces. Another such key design aspect which was used was the starting at the output, and working our way back to the input stage; this meant we were starting with what we wanted, and then determine what we had to do to get to that point. That being said, the final result was quite pleasing to say the least. As the results section highlights, the comparison between the final SPICE model and the actual amplifier show that the circuit performed exactly as expected, with corner frequencies at the 1KHz and 100KHz range, and a gain in the 40-50dB range. Additionally, the triangular wave output shows that distortion really wasn't all that bad, considering the high output amplitude relative to the power rails of only 6V. As a result, the actual amplifier operation was quite successful.

What were the main issues faced then? Or maybe the better question is why did we change to 6V rails versus the original 12V rails the lab started with? The short and simple answer is power dissipation and heat management. Unfortunately, the power transistors used in the lab dissipated a lot of heat when operating on 12V rails, so much so that the heatsinks they were attached to failed to dissipate the heat adequately. When operating the amplifier in this setup, it would run for a very short period of time before going into thermal breakdown, where it failed to operate properly. With, however, the 6V rails, and a bit of circuit modification to accommodate this change, the amplifier worked beautifully, and when measuring the drift when running straight for several minutes, as the lab requested, never really drifted, just deviated around the center point of -26.68mV, which is more than close enough to zero. So, did the amplifier meet specification? Considering that we cut the rail voltage in half, it is reasonable to assume the power requirements should also be halved. If the power requirements are halved (2.5W instead of 5W) then the circuit came extremely close. When looking at the maximum gain of nearly 50dB, which means the output voltage was 9.44Vpp, and a 10Ω load, we have a peak power output current of 0.472A, which means the power was about 2.23A, which, while not quite the desired specification, is quite close, considering the constraints placed in lab due to lack of available components and a poor heatsink. If there were a better heatsink, it is possible the gain would be higher, due to a better dissipation of heat, preventing thermal breakdown.

VII. Appendices

Lengthy tables, excess oscilloscope waveforms, excess computer outputs